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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/695,390	HA ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *20-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/01/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Group I, claims 1-19, in the reply filed on 01/30/2008 is acknowledged. The traversal is on the ground(s) that "there exists enough common and related subject matter in the claims such that it would not be an undue burden for the Examiner to examine all of the claims". This is not found persuasive because claim 21 for Group II requires further search and consideration for a first divider for outputting a maximum integer not exceeding a quotient obtained by dividing an index of a code symbol requested by the channel decoder by 2^m; a BRO operator for grouping bits obtained by dividing the code symbol index by 2^m, and performing a BRO operation on row indexes for symbols of each group; a multiplier for multiplying an output of the BRO operator by (J^{-1}); and a first adder for calculating the interim address by adding an output of the multiplier to an output of the first divider. Claim 28 for Group III requires further search and consideration for A method for performing addressing so as to generate deinterleaved symbols from an input buffer that performs a bit reversal order (BRO) operation on column indexes of symbols in 2^m columns among $(2^m xJ+R)$ symbols, where 2^m is the number of columns, J is the number of columns and R is the number of remaining symbols in a $(J+1)^{th}$ column, and sequentially writes interleaved symbols corresponding to code symbol indexes k, the method comprising the steps of: performing BRO operation of column indexes of the code symbol indexes; generating a interim addresses by adding the BRO operated

column indexes to a column index of the code symbol indexes; generating address compensation factor for compensating addresses of remaining symbols from the code symbol index of $(J+1)^{th}$; and generating addresses by adding the interim address values and the address compensation factors, and applying the addresses to the buffer. And claim 32 of Group IV requires further search and consideration for An apparatus for performing addressing so as to generate deinterleaved symbols from an input buffer that performs a bit reversal order (BRO) operation on column indexes of symbols in 2^m columns among $(2^m xJ+R)$ symbols, where 2^m is the number of columns, J is the number of columns and R is the number of remaining symbols in a $(J+1)^{th}$ column, and sequentially writes interleaved symbols corresponding to code symbol indexes k, the apparatus comprising: an interim address generator for performing BRO operation of column indexes of the code symbol indexes and adding the BRO operated column indexes to a column index of the code symbol indexes; an address compensation factor calculator for generating address compensation factor for compensating addresses of remaining symbols from the code symbol index of $(J+1)^{th}$ column; and an adder for adding output of the interim address generator and output of the address compensation factor calculator.

The requirement is still deemed proper and is therefore made FINAL.

Claims 20-32 withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to nonelected inventions, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 01/30/2008.

Oath/Declaration

The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:
The clause regarding "willful false statements ..." required by 37 CFR 1.68 has been omitted.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: '30', '320a', '320b', '320c', '320d', '472', '320e' and '320f' in Figures 2, 10-15. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 17-19 are objected to because of the following informalities: the language in claims 17-19 lacks antecedent basis in the specification. See MPEP 608.01(o). Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 17-19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Nowhere in the specification does the Applicant teach "performing BRO operation of column indexe of the code symbol indexe; and adding the BRO operated column indexe and a column index of the code symbol indexe". Lines 15-27 of the Applicant's specification instead teach "Since a code symbol first excluded from the last column is always located in a **row index d-1** in the light of a characteristic of a BRO operation, r^{-} is d-1" [Emphasis added].

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 3, 15, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The terms "the $(J+1)^{th}$ column", "the (J+1) column" and "the $(J+1)^{th}$ last column" in claims 2, 3 and 15 lack antecedent basis.

The language in claims 17-19 lacks antecedent basis in the specification

Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01.

As per claim 1: Claim 1 recites, "calculating an address compensation factor for compensating the interim address **in consideration of** the remainder" [Emphasis added]. The relationship between "calculating an address compensation factor" and "the remainder" is unspecified and indefinite.

As per claims 2 and 3: Claim 1 recites, "generating an interim address by bit reversal order (BRO) operation on an index of a code symbol". The relationship between generating an interim address by bit reversal order (BRO) operation and the interim address generation step of claims 2 and 3 is not clear. That is, what does "excluding the $(J+1)^{th}$ column" and "including the $(J+1)^{th}$ column" have to do with "generating an interim address by **bit reversal order (BRO) operation**" [Emphasis added].

As per claim 3: Claim 1 recites, "calculating an address compensation factor for compensating the interim address in consideration of the remainder". The relationship between calculating an address compensation factor for compensating the interim address in consideration of the remainder and address compensation factor calculation step of claim 3 is not clear. That is, what does "increasing the address compensation factor by one..." and "decreasing the address compensation factor by one..." have to do with "calculating an address compensation factor for compensating the interim address **in consideration of the remainder**" [Emphasis added].

As per claim 4: Claim 1 recites "generating an interim address by bit reversal order (BRO) operation on an index of a code symbol; calculating an address compensation factor for compensating the interim address in consideration of the remainder; and generating a read address by adding the interim address to the address compensation factor for the code symbol". The step for "generating a read address" in claim 4 appears to contradict the step for "generating a read address" in claim 1 and, in particular, the relationship between the step for "generating a read address" in claim 4 and the step for "generating a read address" in claim 1 is unspecified and indefinite.

As per claim 5: Claim 1 recites "generating an interim address by bit reversal order (BRO) operation on an index of a code symbol; calculating an address compensation factor for compensating the interim address in consideration of the remainder; and generating a read address by adding the interim address to the address compensation factor for the code symbol". The step for "generating a read address" in claim 5 appears to contradict the step for "generating a read address" in claim 1 and, in

particular, the relationship between the step for "generating a read address" in claim 5 and the step for "generating a read address" in claim 1 is unspecified and indefinite.

As per claim 6: Claim 1 recites "generating an interim address by bit reversal order (BRO) operation on an index of a code symbol; calculating an address compensation factor for compensating the interim address in consideration of the remainder; and generating a read address by adding the interim address to the address compensation factor for the code symbol". The step for "generating a read address" in claim 6 appears to contradict the step for "generating a read address" in claim 1 and, in particular, the relationship between the step for "generating a read address" in claim 6 and the step for "generating a read address" in claim 1 is unspecified and indefinite.

As per claim 7: Claim 1 recites "generating an interim address by bit reversal order (BRO) operation on an index of a code symbol; calculating an address compensation factor for compensating the interim address in consideration of the remainder; and generating a read address by adding the interim address to the address compensation factor for the code symbol". The step for "generating a read address" in claim 7 appears to contradict the step for "generating a read address" in claim 1 and, in particular, the relationship between the step for "generating a read address" in claim 7 and the step for "generating a read address" in claim 1 is unspecified and indefinite.

As per claim 8: Claim 1 recites "generating an interim address by bit reversal order (BRO) operation on an index of a code symbol; calculating an address compensation factor for compensating the interim address in consideration of the remainder; and generating a read address by adding the interim address to the address

compensation factor for the code symbol". The step for "generating a read address" in claim 8 appears to contradict the step for "generating a read address" in claim 1 and, in particular, the relationship between the step for "generating a read address" in claim 8 and the step for "generating a read address" in claim 1 is unspecified and indefinite.

As per claim 9: Claim 1 recites "generating an interim address by bit reversal order (BRO) operation on an index of a code symbol; calculating an address compensation factor for compensating the interim address in consideration of the remainder; and generating a read address by adding the interim address to the address compensation factor for the code symbol". The step for "generating a read address" in claim 9 appears to contradict the step for "generating a read address" in claim 1 and, in particular, the relationship between the step for "generating a read address" in claim 9 and the step for "generating a read address" in claim 1 is unspecified and indefinite.

As per claim 10: Claim 1 recites "generating an interim address by bit reversal order (BRO) operation on an index of a code symbol; calculating an address compensation factor for compensating the interim address in consideration of the remainder; and generating a read address by adding the interim address to the address compensation factor for the code symbol". The step for "generating a read address" in claim 10 appears to contradict the step for "generating a read address" in claim 1 and, in particular, the relationship between the step for "generating a read address" in claim 10 and the step for "generating a read address" in claim 1 is unspecified and indefinite.

As per claim 11: Claim 1 recites "generating an interim address by bit reversal order (BRO) operation on an index of a code symbol; calculating an address

compensation factor for compensating the interim address in consideration of the remainder; and generating a read address by adding the interim address to the address compensation factor for the code symbol". The step for "generating a read address" in claim 11 appears to contradict the step for "generating a read address" in claim 1 and, in particular, the relationship between the step for "generating a read address" in claim 11 and the step for "generating a read address" in claim 1 is unspecified and indefinite.

As per claim 12: Claim 1 recites "generating an interim address by bit reversal order (BRO) operation on an index of a code symbol; calculating an address compensation factor for compensating the interim address in consideration of the remainder; and generating a read address by adding the interim address to the address compensation factor for the code symbol". The step for "generating a read address" in claim 12 appears to contradict the step for "generating a read address" in claim 1 and, in particular, the relationship between the step for "generating a read address" in claim 12 and the step for "generating a read address" in claim 1 is unspecified and indefinite.

As per claim 13: Claim 1 recites "generating an interim address by bit reversal order (BRO) operation on an index of a code symbol; calculating an address compensation factor for compensating the interim address in consideration of the remainder; and generating a read address by adding the interim address to the address compensation factor for the code symbol". The step for "generating a read address" in claim 13 appears to contradict the step for "generating a read address" in claim 1 and, in particular, the relationship between the step for "generating a read address" in claim 13 and the step for "generating a read address" in claim 1 is unspecified and indefinite.

As per claim 14: Claim 1 recites "generating an interim address by bit reversal order (BRO) operation on an index of a code symbol; calculating an address compensation factor for compensating the interim address in consideration of the remainder; and generating a read address by adding the interim address to the address compensation factor for the code symbol". The step for "generating a read address" in claim 14 appears to contradict the step for "generating a read address" in claim 1 and, in particular, the relationship between the step for "generating a read address" in claim 14 and the step for "generating a read address" in claim 1 is unspecified and indefinite.

As per claim 15: Claim 1 recites "an interleaved encoder packet has (2^m*J+R) bits, a bit shift value m, an up-limit value J and a remainder R, the method comprising the steps of"... "calculating an address compensation factor for compensating the interim address in consideration of the remainder". The step for "calculating an address compensation factor" in claim 15 appears to contradict the step for "calculating an address compensation factor" in claim 1 and, in particular, the relationship between the step for "calculating an address compensation factor" in claim 15 and the step for "calculating an address compensation factor" in claim 1 is unspecified and indefinite.

As per claim 16: Claim 1 recites "an interleaved encoder packet has (2^m*J+R) bits, a bit shift value m, an up-limit value J and a remainder R, the method comprising the steps of"... "calculating an address compensation factor for compensating the interim address in consideration of the remainder". The step for "calculating an address compensation factor" in claim 16 appears to contradict the step for "calculating an address compensation factor" in claim 1 and, in particular, the relationship between the

step for "calculating an address compensation factor" in claim 16 and the step for "calculating an address compensation factor" in claim 1 is unspecified and indefinite.

As per claim 17: Claim 1 recites "generating an interim address by bit reversal order (BRO) operation on an index of a code symbol". The step for "generating an interim address" in claim 17 appears to contradict the step for "generating an interim address" in claim 1 and, in particular, the relationship between the step for "column indexe" in claim 17 and the "symbol index" in claim 1 is unspecified and indefinite.

As per claim 18: It is not clear how the recited column index figures into the dividing calculation of the code symbols.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-19 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 1 recites, "A method for reading code symbols" in the preamble.

The limitations in claim 1 are directed to an abstract mathematical algorithm of generating an abstract binary address number value intended for use in a abstract method for reading data intended for use in implementing an abstract algorithm for rearranging data.

The claims as written attempt to gain a patent on every "substantial practical application" of an abstract mathematical algorithm/idea.

The courts have also held that a claim may not preempt< ideas, laws of nature or natural phenomena. The concern over preemption was expressed as early as 1852. See Le Roy v. Tatham, 55 U.S. 156, 175 (1852) ("A principle, in the abstract, is a fundamental truth; an original cause; a motive; these cannot be patented, as no one can claim in either of them an exclusive right."); Funk Brothers Seed Co. v. Kalo Inoculant Co., 333 U.S. 127, 132, 76 USPQ 280, 282 (1948) (combination of six species of bacteria held to be nonstatutory subject matter).

**>Accordingly, one may not patent every "substantial practical application" of an idea, law of nature or natural phenomena because such a patent would "in practical effect be a patent on the [idea, law of nature or natural phenomena] itself." Gottschalk v. Benson, 409 U.S. 63, 71-72, 175 USPQ 673, 676 (1972).

Simply put, claims that describe features in the Applicant's specification at the Abstract level without any regard to function or utility are nonstatutory.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, are rejected under 35 U.S.C. 102(b) as being anticipated by KIM M et al. (WO 0035102 A 1, hereafter referred to as Kim).

35 U.S.C. 102(b) rejection of claim 1.

Kim clearly suggests generating an interim address by bit reversal order, BRO, operation on an index of a code symbol (BRO(K/J) on page 3 of Kim is an interim address of a bit reversal order, BRO, operation on an index of a code symbol); calculating an address compensation factor for compensating the interim address in consideration of the remainder (2^m(K mod J) on page 3 of Kim is an address compensation factor for compensating the interim address in consideration of the remainder K mod J); and generating a read address by adding the interim address to the address compensation factor for the code symbol (BRO(K/J) + (2^m(K mod J) on page 3 of Kim is a read address calculated by adding the interim address (BRO(K/J) to the address compensation factor (2^m(K mod J) for the code symbol), and reading the code symbol written in the generated read address (Figure 2 of Kim).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to

be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 1 is rejected on the ground of nonstatutory double patenting over claim 1 of U. S. Patent No. US 6668350 B1 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows: claim 1 of U. S. Patent No. US 6668350 B1 clearly suggests generating an interim address by bit reversal order, BRO, operation on an index of a code symbol (BRO(K/J) is an interim address of a bit reversal order, BRO, operation on an index of a code symbol); calculating an address compensation factor for compensating the interim address in consideration of the remainder (2^m(K mod J) is an address compensation factor for compensating the interim address in consideration of the remainder K mod J); and generating a read address by adding the interim address to the address compensation factor for the code symbol (BRO(K/J) + (2^m(K mod J) is a read address calculated by adding the interim address (BRO(K/J) to the address compensation factor (2^m(K mod J) for the code symbol).

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Art Unit 2112

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